PATENT ABSTRACTS OF JAPAN

(11) Publication number:

06-275718

(43) Date of publication of application: 30.09.1994

(51)Int.Cl.

HO1L 21/82

HO1L 27/118

(21)Application number : **05-059777**

(71)Applicant: TOSHIBA CORP

(22) Date of filing:

19.03.1993

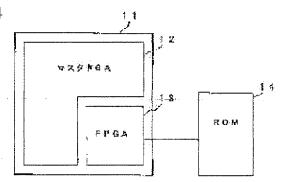
(72)Inventor: NIIFUNA TAKEO

(54) GATE ARRAY CIRCUIT

(57) Abstract:

PURPOSE: To utilize both advantages of fast operating speed and many number of gates of a masked gate array and programmability of a desired circuit by the user of FPGA.

CONSTITUTION: A masked gate array (GA) 12 and an SRAM type FPGA are provided in the same ASIC chip 11, and a RAM 14 as a nonvolatile memory for storing wiring information of the FPGA is connected to the chip 11.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]